DOCUMENT NUMBER AND REVISION

VL-PS-COG-TA25F325P-L5 REV.A

(COG-TA25F325P-L5)

DOCUMENT TITLE:

PRELIMINARY SPECIFICATION

OF

TFT MODULE TYPE

CUSTOMER	
CUSTOMER REFERENCE NO.	**N/A**
MODEL NUMBER	**COG-TA25F325P-L5**
CUSTOMER APPROVAL	
DATE	

DEPARTMENT	NAME	SIGNATURE	DATE
PREPARED BY	LI TING		
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APPROVED BY TFT EE	LI ZHAO FA/ DEVIN DENG		
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A	2019.09.02	First Release.	LI TING	LI JIAN LUN

CONTENTS

BOE VARITRONIX LIMITED

Preliminary Specification
Of
TFT Module Type
Model No.: COG-TA25F325P-L5

1. General Description

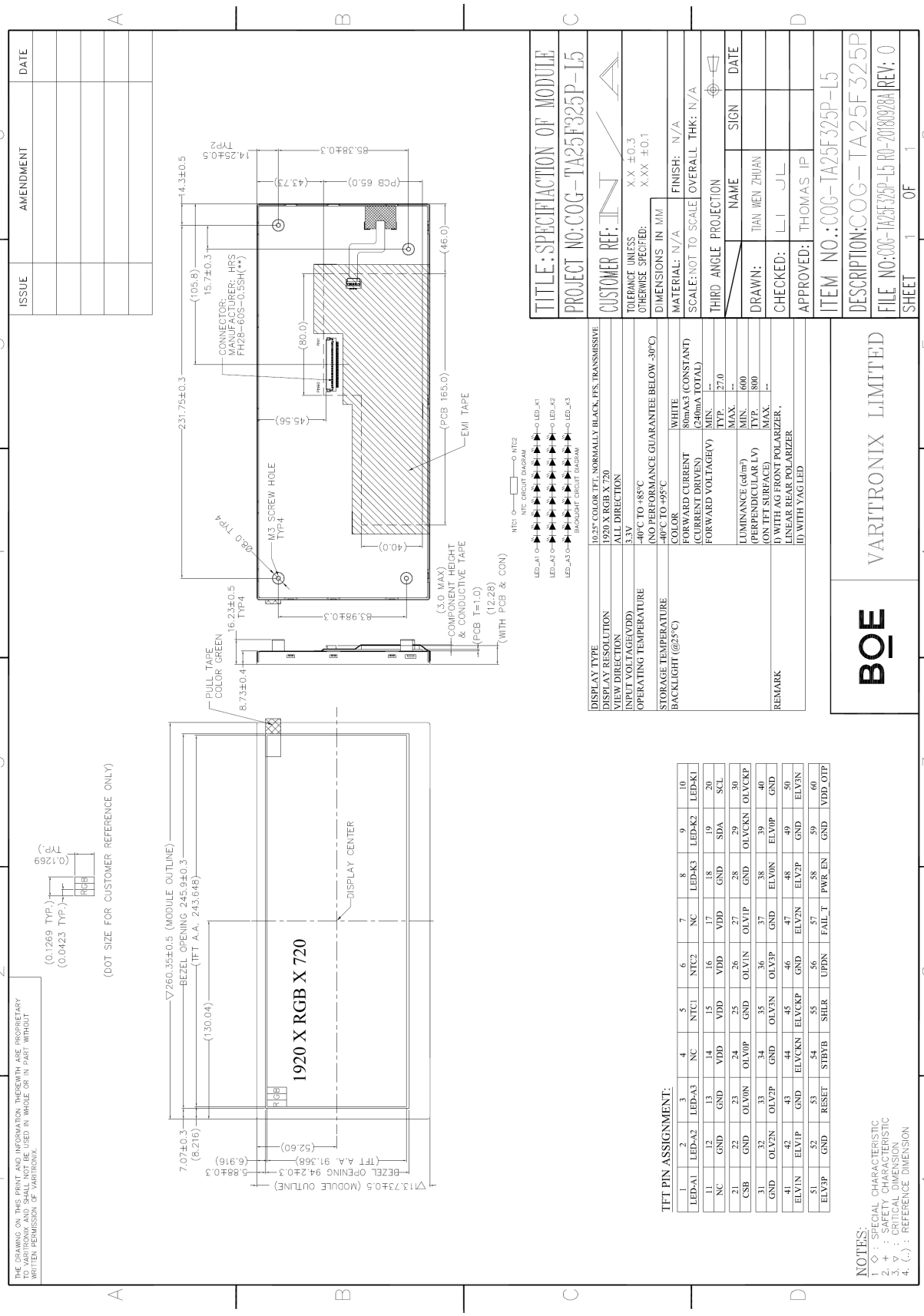
- 10.25" (diagonal), 8:3, Landscape, Transmissive, Normally black, Amorphous silicon TFT LCD module
- Display resolution: 1920 x RGB x 720
- Viewing direction: All direction
- LVDS interface
- TFT-LCD logic voltage (VDD): 3.3V (TYP.)
- With front bezel, AG POL
- YAG LED
- “RoHS” compliance.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1: Module mechanical detail

Parameters		Specifications	Unit
Outline dimensions		260.35(W) x 113.73(H) x 8.73(D) (Exclude FPC, cables & component and mounting screws)	mm
Color TFT 1920 x RGB x 720	Active area	243.648(W) x 91.368(H)	mm
	Display format	1920 x RGB x 720	dots
	Color configuration	RGB vertical stripes	-
	Dot pitch	0.0423 (*3) (W) x 0.1269(H)	mm
Backlight		White LED	-
Weight		374	gram



DISPLAY TYPE	10.25" COLOR TFT, NORMALLY BLACK, FFS, TRANSMISSIVE		
DISPLAY RESOLUTION	1920 X RGB X 720		
VIEW DIRECTION	ALL DIRECTION		
INPUT VOLTAGE(VDD)	3.3V		
OPERATING TEMPERATURE	-40°C TO +85°C (NO PERFORMANCE GUARANTEE BELOW -30°C)		
STORAGE TEMPERATURE	-40°C TO +95°C		
BACKLIGHT (@25°C)	COLOR	WHITE	
	FORWARD CURRENT (CURRENT DRIVEN)	80mAx3 (CONSTANT) (240mA TOTAL)	
	FORWARD VOLTAGE(V)	MIN.	--
		TYP.	27.0
		MAX.	--
	LUMINANCE (cd/m²) (PERPENDICULAR LV) (ON TFT SURFACE)	MIN.	600
		TYP.	800
		MAX.	--
REMARK	1) WITH AG FRONT POLARIZER, LINEAR REAR POLARIZER II) WITH YAG LED		

MATERIAL: N/A	FINISH: N/A
SCALE: NOT TO SCALE	OVERALL THK: N/A
THIRD ANGLE PROJECTION	

	NAME	SIGN	DATE
DRAWN:	TIAN WEN ZHUAN		
CHECKED:	LI JL		
APPROVED:	THOMAS IP		

TOLERANCE UNLESS OTHERWISE SPECIFIED: X.X ±0.3, X.XX ±0.1
DIMENSIONS IN MM

ISSUE	AMENDMENT	DATE

TFT PIN ASSIGNMENT:

1	2	3	4	5	6	7	8	9	10
LED-A1	LED-A2	LED-A3	NC	NTC1	NTC2	NC	LED-K3	LED-K2	LED-K1
11	12	13	14	15	16	17	18	19	20
NC	GND	GND	VDD	VDD	VDD	VDD	GND	SDA	SCL
21	22	23	24	25	26	27	28	29	30
CSB	GND	OLV0N	OLV0P	GND	OLV1N	OLV1P	GND	OLVCKN	OLVCKP
31	32	33	34	35	36	37	38	39	40
GND	OLV2N	OLV2P	GND	OLV3N	OLV3P	GND	ELV0N	ELV0P	GND
41	42	43	44	45	46	47	48	49	50
ELV1N	ELV1P	GND	ELVCKN	ELVCKP	GND	ELV2N	ELV2P	GND	ELV3N
51	52	53	54	55	56	57	58	59	60
ELV3P	GND	RESET	STBYB	SHLR	UPDN	FAIL_T	PWR_EN	GND	VDD_OTP

NOTES:
1. ◇ : SPECIAL CHARACTERISTIC
2. + : SAFETY CHARACTERISTIC
3. ▽ : CRITICAL DIMENSION
4. (..) : REFERENCE DIMENSION

Figure 1: Module specification

3. Interface Signals

Table 2

Pin No.	Symbol	I/O	Description	Remarks
1	LED-A1	P	LED Anode	
2	LED-A2	P	LED Anode	
3	LED-A3	P	LED Anode	
4	NC	-		
5	NTC1	C	NTC thermistor terminal 2	
6	NTC2	C	NTC thermistor terminal 2	
7	NC	-		
8	LED-K3	P	LED string 3 Cathode	
9	LED-K2	P	LED string 2 Cathode	
10	LED-K1	P	LED string 1 Cathode	
11	NC	-		
12	GND	P	Ground	
13	GND	P	Ground	
14	VDD	P	Power pin for Logic	3.3V typ.
15	VDD	P	Power pin for Logic	3.3V typ.
16	VDD	P	Power pin for Logic	3.3V typ.
17	VDD	P	Power pin for Logic	3.3V typ.
18	GND	P	Ground	
19	SDA	I/O	SPI Data pin	L: When not use
20	SCL	I	SPI Clock pin	L: When not use
21	CSB	I	SPI Chip Select Enable pin	H: When not use
22	GND	P	Ground	
23	OLV0N	I	Odd Data channel 0-	
24	OLV0P	I	Odd Data channel 0+	
25	GND	P	Ground	
26	OLV1N	I	Odd Data channel 1-	
27	OLV1P	I	Odd Data channel 1+	
28	GND	P	Ground	
29	OLVCKN	I	Odd Clock channel -	
30	OLVCKP	I	Odd Clock channel +	
31	GND	P	Ground	
32	LOV2N	I	Odd Data channel 2-	
33	LOV2P	I	Odd Data channel 2+	
34	GND	P	Ground	
35	LOV3N	I	Odd Data channel 3-	
36	LOV3P	I	Odd Data channel 3+	
37	GND	P	Ground	
38	ELV0N	I	Even Data channel 0-	
39	ELV0P	I	Even Data channel 0+	
40	GND	P	Ground	
41	ELV1N	I	Even Data channel 1-	

Pin No.	Symbol	I/O	Description	Remarks
42	ELV1P	I	Even Data channel 1+	
43	GND	P	Ground	
44	ELVCKN	I	Even Clock channel -	
45	ELVCKP	I	Even Clock channel +	
46	GND	P	Ground	
47	ELV2N	I	Even Data channel 2-	
48	ELV2P	I	Even Data channel 2+	
49	GND	P	Ground	
50	ELV3N	I	Even Data channel 3-	
51	ELV3P	I	Even Data channel 3+	
52	GND	P	Ground	
53	RESET	I	Reset Pin	L:Reset H:Normal
54	STBYB	I	Standby Pin	L:Reset H:Normal
55	SHLR	I	Horizontal Shift Direction Selection	
56	UPDN	I	Vertical Shift Direction Selection	
57	FALL_T	O	Failure Detect output pin	FAIL_DET = H when Module with detected failure mode. Read failure mode through SPI FAIL_DET = L: Normal
58	PWR_EN	-	NC	
59	GND	P	Ground	
60	VDD_OTP	I	Power input for OTP	User set it to 3.3V

Remarks: For I/O, “I” is Input, “O” is Output. “P” is for Power, and “C” is for passive.

Note 1: This pin contains the RC circuit, R=10K, C=1uF.

Note 2: This pin contains the RC circuit, R=10K, C=2.2uF.

Note 3: NTC: Murata NCP18XH103F0SRB, Typ. 10.0kΩ +/-1% at 25°C.

4. Absolute Maximum Ratings

The product or its functions may subject to permanent damage if it's stressed beyond those absolute maximum ratings listed below. Exposure to absolute maximum rating conditions for extended periods may affect display module reliability.

Table 3: Absolute Maximum Ratings & Environmental Conditions

Item	Symbol	Min.	Max.	Unit
Digital supply voltage	VDD	-0.3	+3.96	V
DCDC supply voltage	VDDA	-0.3	+3.96	V
Digital I/O input signals	V_{IO}	-0.3	VDD+0.3	V
Single LED forward current	I_F	-	80	mA
Total LED forward current	I_F (Total)	-	240	mA
Relative Humidity (at 60°C)	RH	-	90	%
Operating Temperature (Note 2)	Topr	-40	+85	°C
Storage Temperature	Tstg	-40	+95	°C

Note 1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Note 2: Optical deviation under -30^{o}C

Note 3: Panel surface temperature should not exceed 95°C. No performance guarantee below -30°C.

Note 4: No condensation allowed under any condition.

[Caution]

Do not display fixed pattern for prolonged hours because it may develop image sticking on the display.

5. Electrical Specifications

5.1 Block Diagram

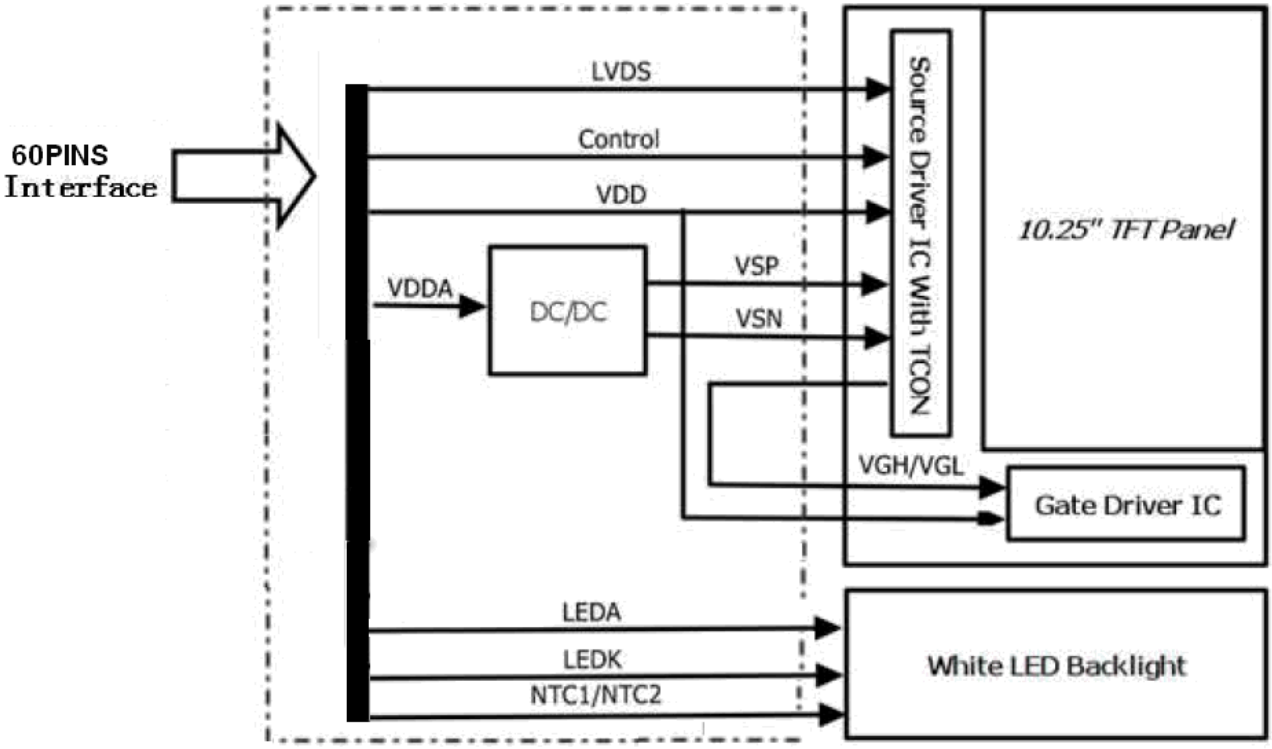


Figure 2: Block diagram

5.2 Typical Electrical Characteristics for TFT-LCD

At Ta = 25 °C, DVDD=3.3V, DGND=0V

Table 4: DC characteristics for TFT-LCD

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage for DCDC	VDDA	3.0	3.3	3.6	V
Power supply voltage for Logic	VDD	3.0	3.3	3.6	V
Power supply current for DCDC	IVDDA (Note 2)	-	400	600	mA
Power supply current for Logic	IDD (Note 2)	-	40	60	mA
Driver input high signal voltage	V_{IH}	0.7*VCC	-	VCC	V
Driver input low signal voltage	V_{IL}	GND	-	0.3*VCC	V
LED Life Time (50%)	(Note 3)	30000	-	-	hrs

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

Note 2: All white pattern.

Note 3: The “LED Life Time” is defined as the time period when the brightness decrease to 50% of the initial value under continuous lighting at 25°C (dry condition) with the recommended driving current

Table 5: LVDS DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Differential input high Threshold voltage	V_{TH}	-	-	+0.1	V
Differential input low threshold voltage	V_{TL}	-0.1	-	-	V
Differential input common Mode voltage	V_{CM}	1	1.2	1.8-| V_{ID} |/2	V
LVDS input voltage	V_{INLV}	0.7	-	1.8	V
Differential input voltage	| V_{ID} |	0.2	-	0.6	V
Differential input leakage Current	Ilv leak	-10	-	+10	uA

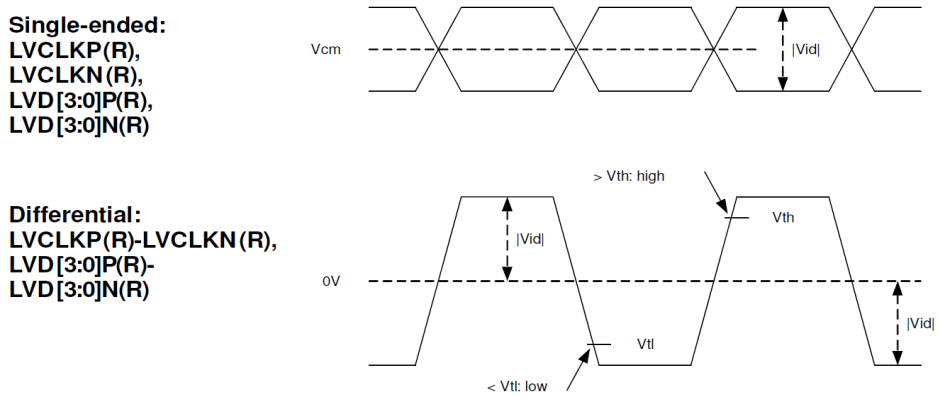


Figure 3

5.3 Recommended Driving Condition for LED Backlight

Table 6: DC characteristics of LED backlight

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Supply voltage of LED backlight	V_{LED}	Backlight current = 240mA Number of LED dies = 30 pcs	-	27.0	-	V	Note 1
Supply current of LED backlight	$I_{LED1/3}$	Per LED string	-	80	-	mA	Note 2
Total Supply current of LED backlight	$I_{LEDTotal}$	$I_{LED1} + \ldots + I_{LED3}$	-	240	-	mA	Note 2
Backlight Power Consumption	P_{LED}	-	-	6.48	-	W	Note 3

Note 1: Backlight Circuit Diagram

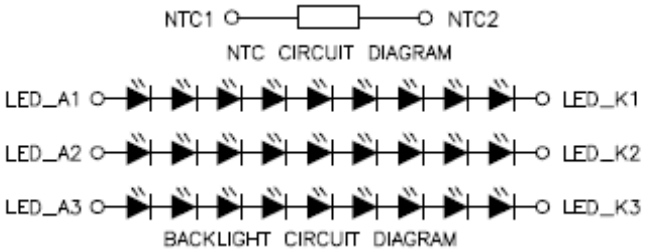


Figure 4: LED circuit diagram

Note 2: The LED driving condition is defined for each LED module.
Total input current = 80 x 3= 240mA

Note 3: Backlight power consumption is calculated by I_{LED} (Total) x V_{LED}

Note 4: The LED Life-time was defined as the estimated time to 50% degradation of initial luminous.

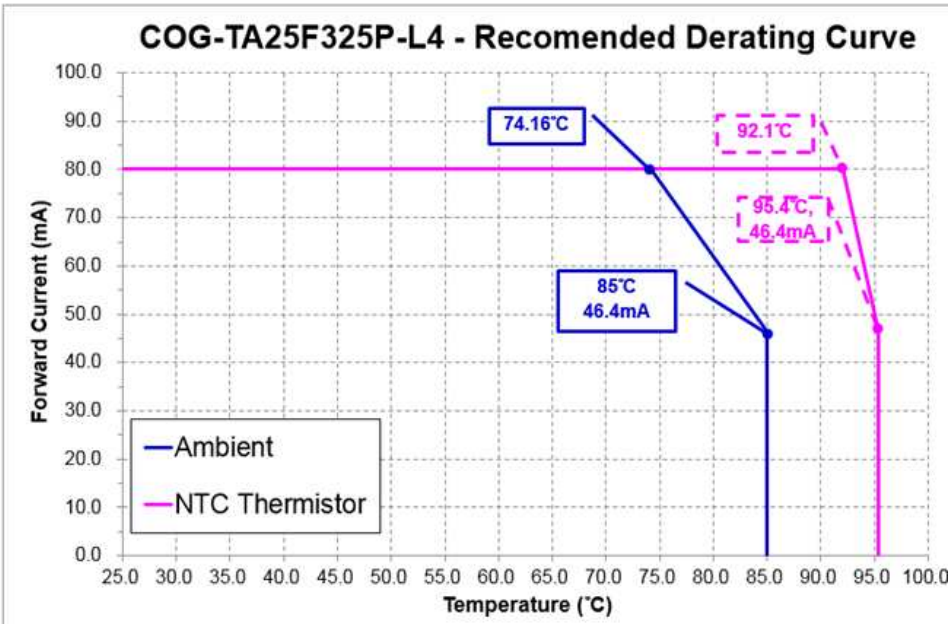


Figure 5: LED driving duty derating curve

5.4 TFT-LCD Timing Characteristics

5.4.1 LVDS AC electrical characteristics

Table 7: AC Characteristic of LVDS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	F_{LVCYC}	20	-	85	MHz
Clock period	T_{LVCYC}	11.76	-	-	ns
1 data bit time	UI	-	1/7	-	T_{LVCYC}
Clock high time	TLVCH	3.9	4	4.1	UI
Clock low time	TLVCL	2.9	3	3.1	UI
Position 1	T_{POS1}	-0.2	0	0.2	UI
Position 0	T_{POS0}	0.8	1	1.2	UI
Position 6	T_{POS6}	1.8	2	2.2	UI
Position 5	T_{POS5}	2.8	3	3.2	UI
Position 4	T_{POS4}	3.8	4	4.2	UI
Position 3	T_{POS3}	4.8	5	5.2	UI
Position 2	T_{POS2}	5.8	6	6.2	UI
Input eye width	T_{EYEW}	0.6	-	-	UI
Input eye border	T_{EX}	-	-	0.2	UI
LVDS wake up time	T_{ENLVDS}	-	-	150	us

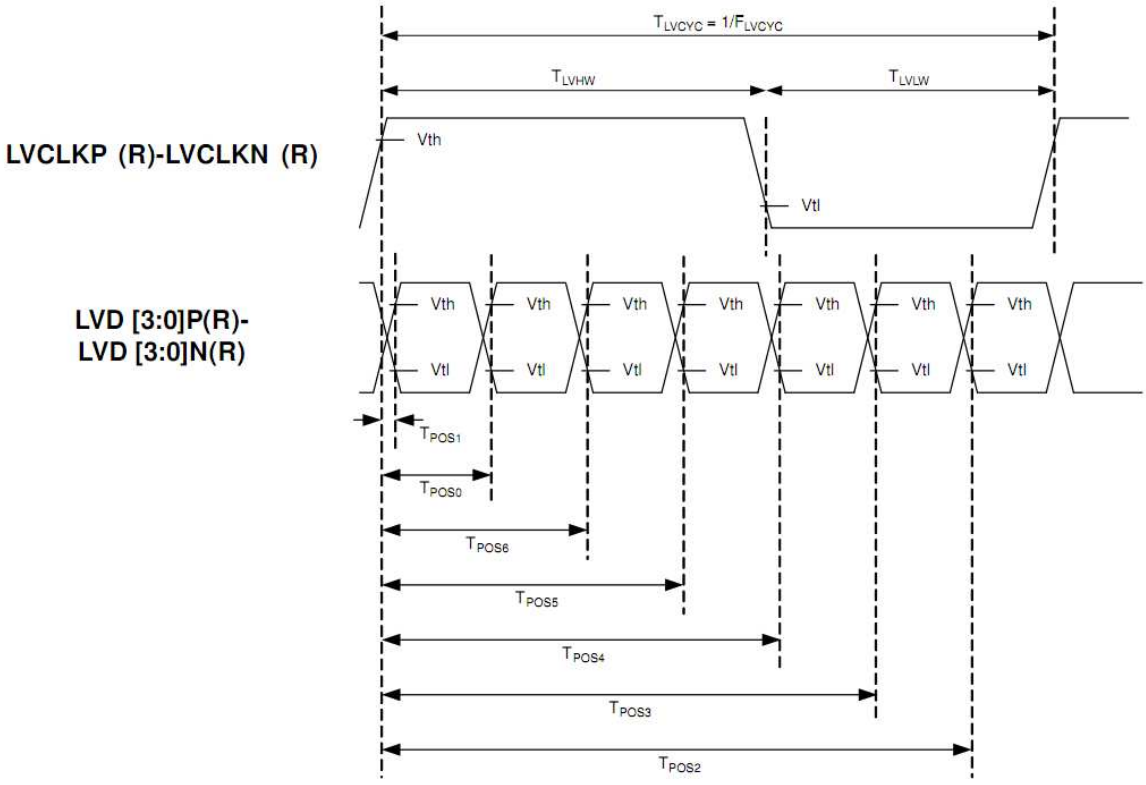


Figure 6(a)

Single-ended:
LVD[3:0]P,
LVD[3:0]N

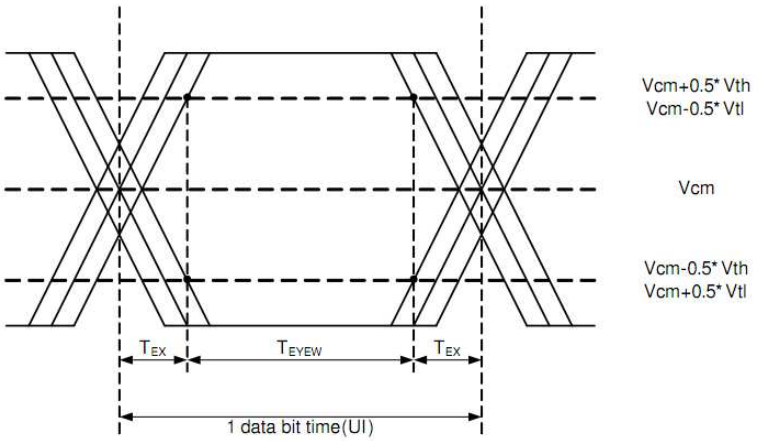


Figure 6(b)

Differential:
LVD[3:0]P-LVD[3:0]N

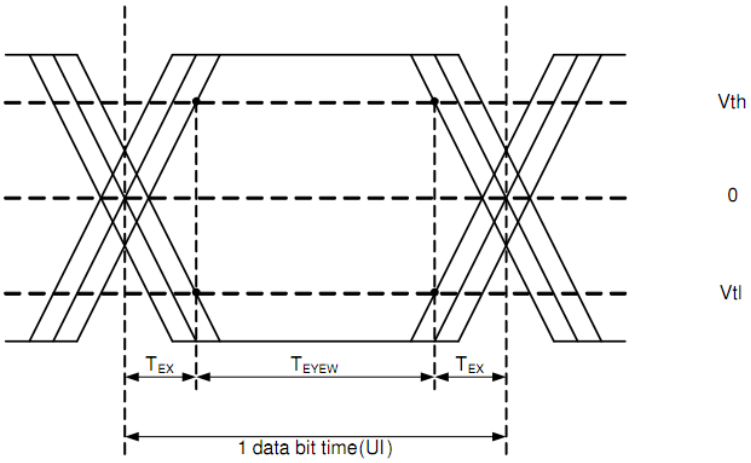


Figure 6(c)

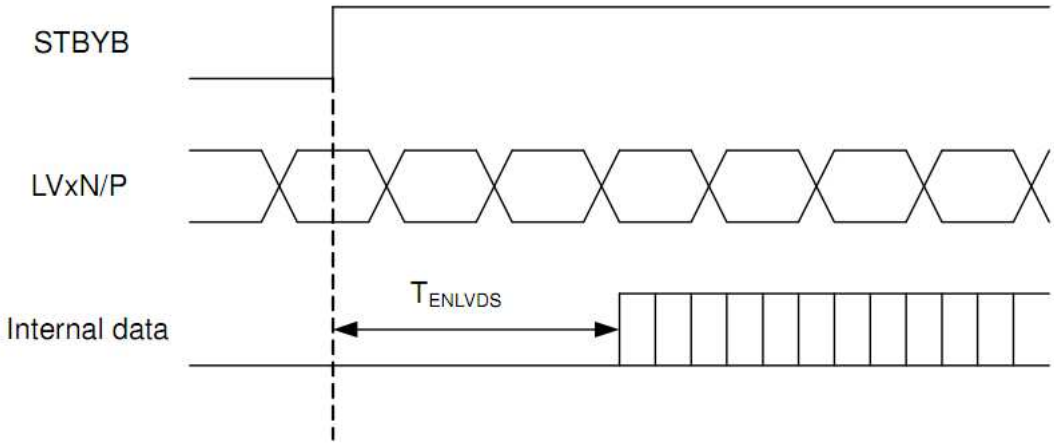


Figure 6(d)

5.4.2 LVDS Input Format (DE mode)

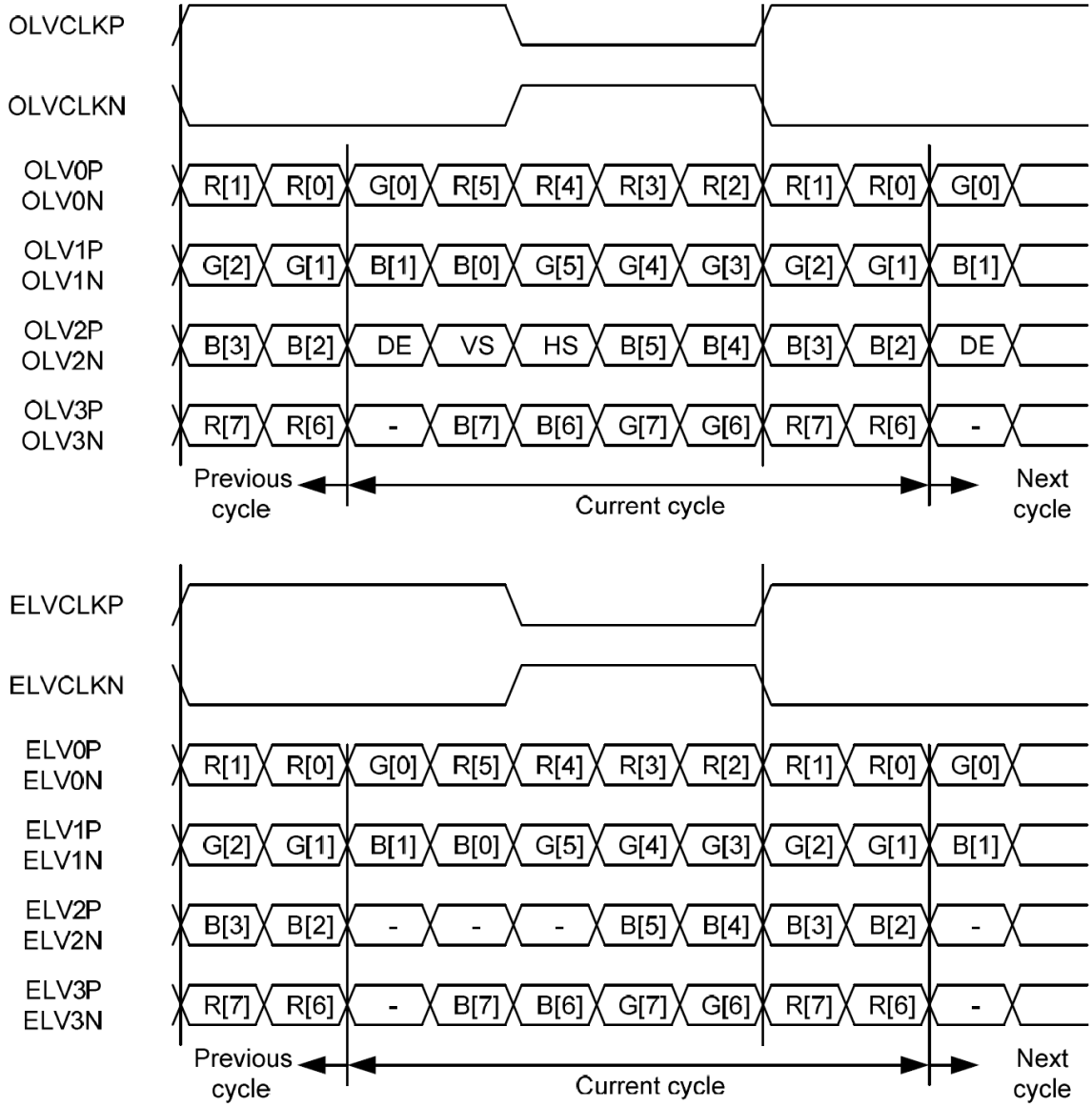


Figure 7: 2-port LVDS signals, VESA format, 8-bit mode

5.4.3 Video Signal Timing

Table 8: Video signal timing

Symbol	Parameter	Conditions	Related Pins	Min.	Typ.	Max.	Unit
VP	Vertical Total	-	VSYNC	728	760	1080	Line
VS	VSYNC Low Pulse Width	-	VSYNC	1	3	254	Line
VBP	Vertical Back Porch	-	VSYNC	2	24	255	Line
VFP	Vertical Front Porch	-	VSYNC	6	16	-	Line
VBL	Vertical Blank period	VFP+VBP	VSYNC	8	40	-	Line
VDISP	Vertical Active Area	-	VSYNC, HSYNC	-	720	-	Line
HP	Horizontal Total		HSYNC	1015	1032	1440	DCK
HS	HSYNC Low Pulse Width	-	HSYNC	6	12	254	DCK
HBP	Horizontal Back Porch	-	HSYNC	5	16	255	DCK
HFP	Horizontal Front Porch	-	HSYNC	50	56	-	DCK
HBLK	Horizontal Blank period	HFP+HBP	HSYNC	55	72	-	DCK
HDISP	Horizontal Active Area	-	HSYNC	-	960	-	DCK
F_{frame}	Frame Frequency	-	CLK	-	60	-	Hz
f_{CLK}	CLK frequency		CLK	-	47.06	-	MHz

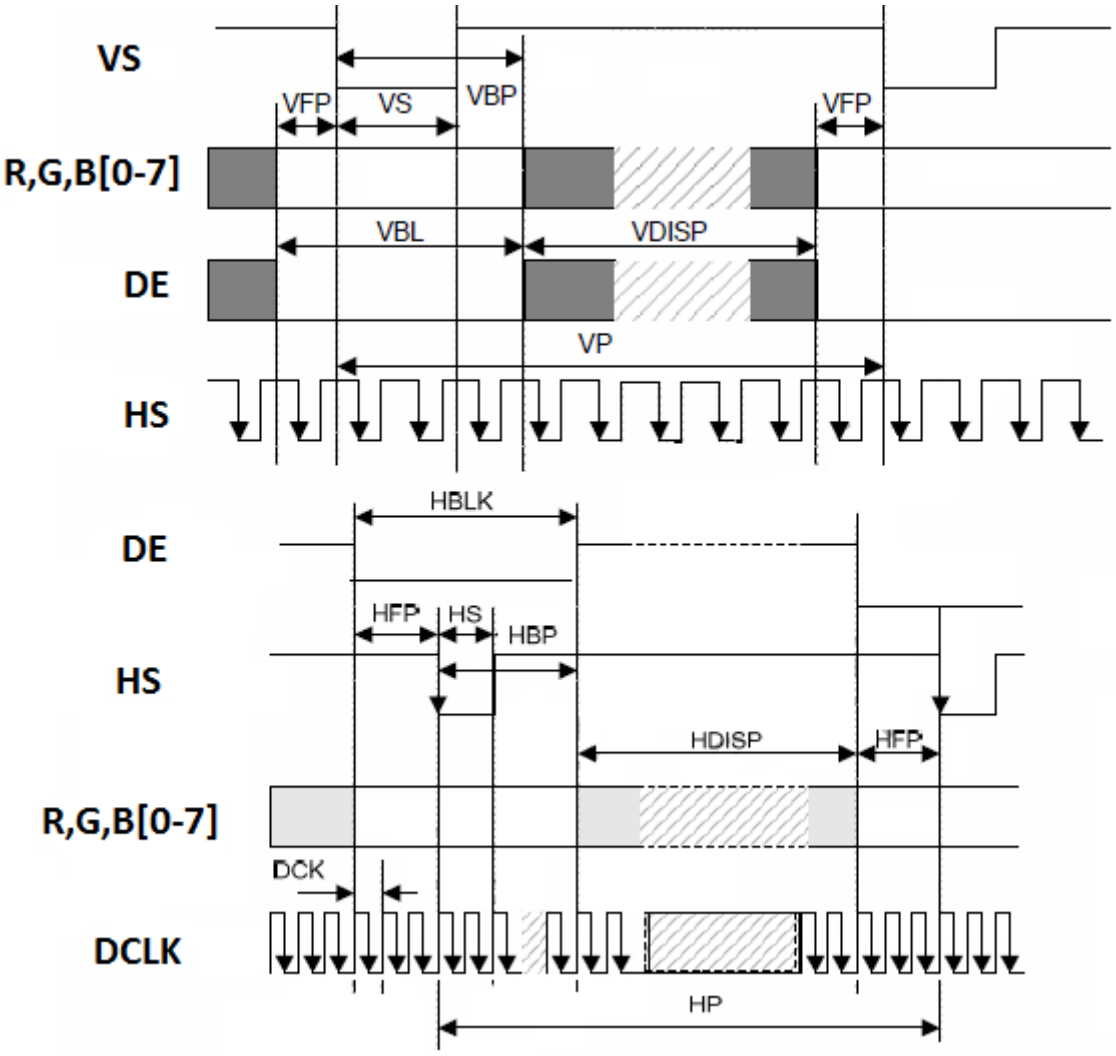


Figure 8

5.4.4 SPI interface (3 wires)

SPI interface is used to read and write the setting registers of the TFT module and read commands to control the TFT module. Refer to Appendix is for details of the registers setting.

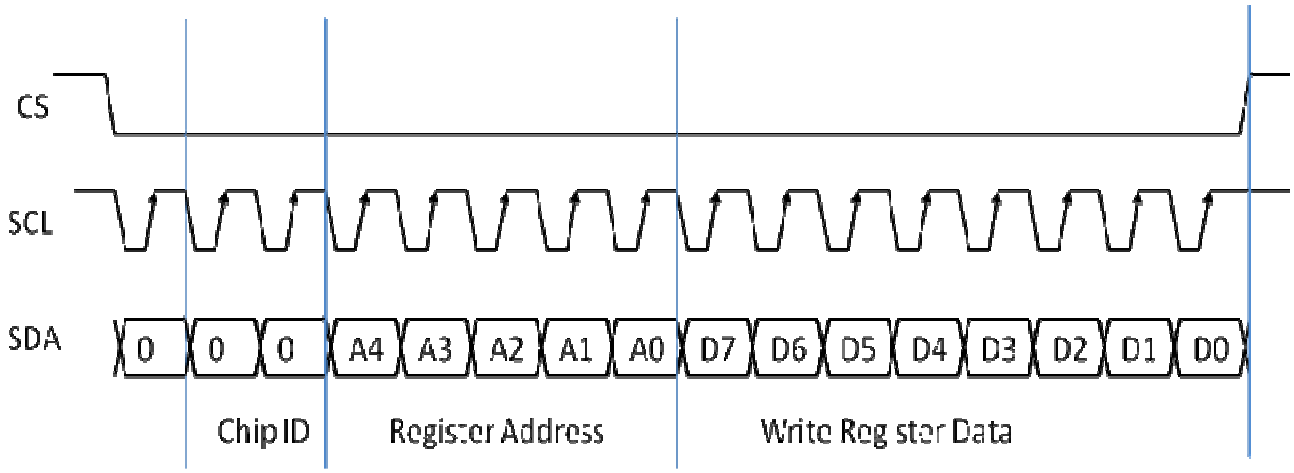


Figure 9(a): SPI write data format

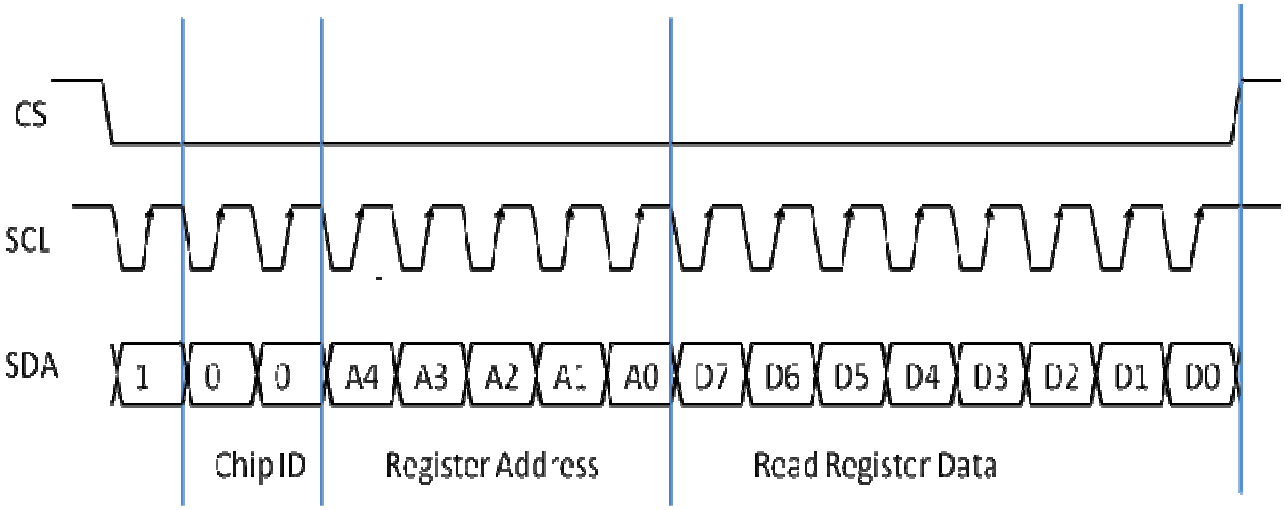


Figure 9(b): SPI read data format

5.4.5 SPI interface timing chart

Table 9: AC Characteristic of SPI Interface

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
SDAI Setup Time	t_{S0}	CSB to SCL	60	-	-	ns
	t_{S1}	SDAI to SCL	60	-	-	ns
SDAI Hold Time	t_{H0}	CSB to SCL	60	-	-	ns
	t_{H1}	SDAI to SCL	60	-	-	ns
Pulse Width	t_{W1L}	SCL pulse width	100	-	-	ns
	t_{W1H}	SCL pulse width	100	-	-	ns
	t_{W2}	CSB pulse width	1	-	-	μs
Clock duty	-	-	40	50	60	%

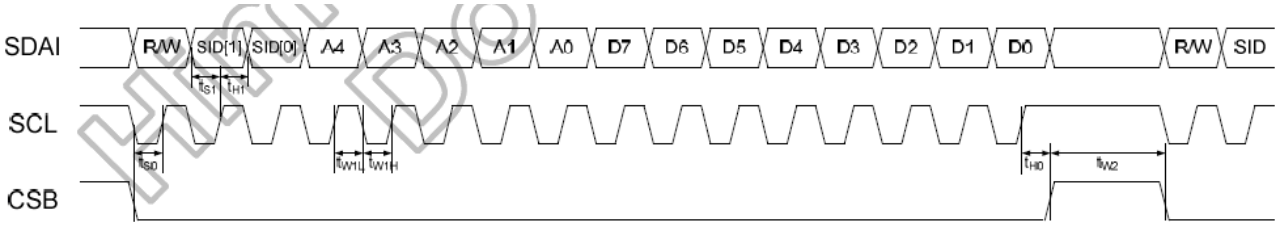
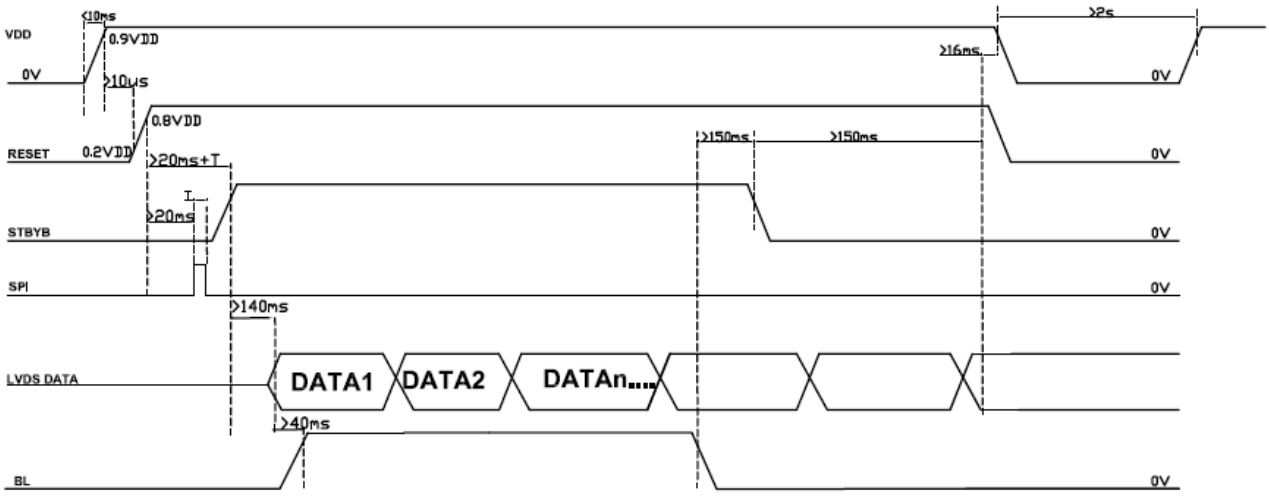


Figure 10: SPI timing

5.5 Power On / Off Sequence



Notes:
1、Abnormal power on/off sequence, maybe lead to abnormal display or TFT module damage..
2、If LVDS signals were out of spec, maybe lead to abnormal display or TFT module damage..

Figure 11: Power on/off sequence

6. Optical Characteristics

Conditions unless specified otherwise:

- Ta = 25°C, dark room
- TFT-LCD supply voltage = 3.3 volts
- Elapsed time from switch on is greater than 30 minutes
- RGB, white and black test patterns only
- Factory settings
- Luminance = 100% unless specified
- Measurements are conducted at ambient temperature and perpendicular unless specified

Table 10: Optical characteristics

Items		Symbol	Condition		Min.	Typ.	Max.	Unit	Note
Response Time		T_R+T_F	Ta = 25°C	Viewing normal angle θ=ϕ=0°	-	21	30	ms	(Note 1)
			Ta =-30°C		-	300	500	ms	
Viewing Angle (Centre)	12’	θ2	Ta=25°C CR > 10		80	85	-	deg	(Note 2)
	6’	θ1			80	85	-		
	9’	ϕ2			80	85	-		
	3’	ϕ1			80	85	-		
Contrast Ratio		CR	Ta=25°C	Viewing normal angle θ=ϕ=0°	900	1068	-	-	(Note 3)
Chromaticity	White	x_W	Ta=25°C		0.275	0.305	0.335	-	(Note 4)
		y_W			0.300	0.330	0.360	-	
	Red	x_R			0.600	0.630	0.660	-	
		y_R			0.302	0.332	0.362	-	
	Green	x_G			0.287	0.317	0.347	-	
		y_G			0.602	0.632	0.662	-	
	Blue	x_B			0.119	0.149	0.179	-	
		y_B			0.029	0.059	0.089	-	
Brightness		L			600	800	-	cd/m2	
Luminance Uniformity		ΔY9	Ta=25°C	9 Points	75	85	-	%	(Note 5)
NTSC Ratio		-	Ta=25°C	-	65	73	-	-	%
Gamma		-	Ta=25°C	-	1.9	2.2	2.5	-	
Flicker		-	50%Gray pattern	-	-	12	18	%	Contrast mode
Reflector Ratio (SCI)		-	Ta=25°C	-	-	5.5	6	%	

Note 1: The electro-optical response time measurements shall be made as FIG. 8 by switching the “data” input signal OFF and ON. The times needed for the luminance to change from 10% to 90% s T_r, and 90% to 10% is T_f.

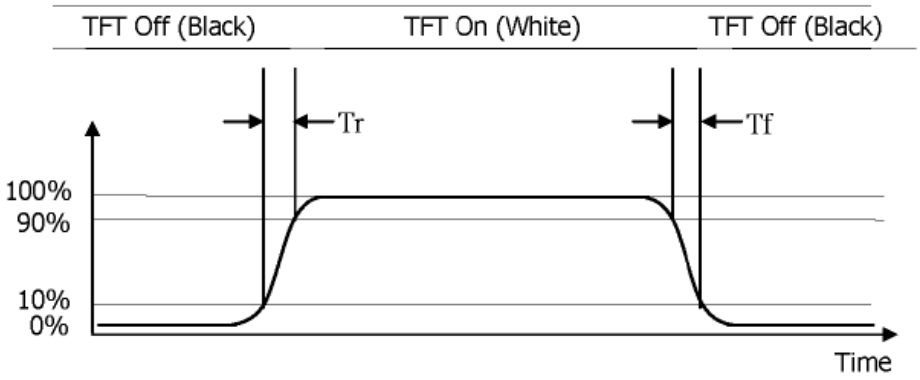


Figure 12: Response Time Testing

Note 2: The definitions of viewing angle.

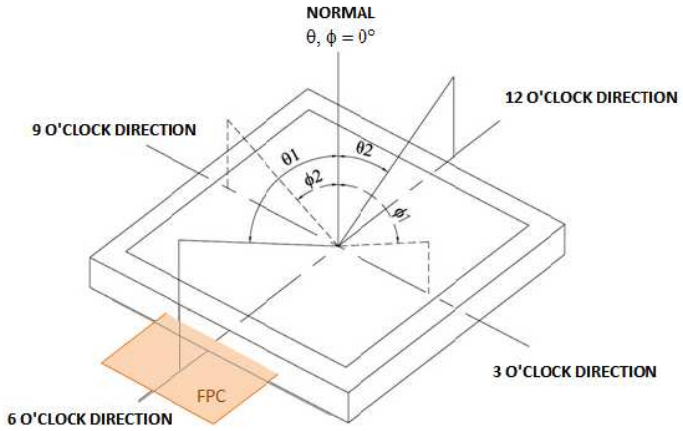


Figure 13: ISO-Contrast Plot (for reference) (Ta = 25°C)

Note 3: Contrast measurements shall be made at viewing angle of $\theta=0^{o}$ and at the center of the LCD surface by using DMS. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state.

Luminace Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note 4: The color chromaticity coordinates specified in Table 10 shall be updated from later actual spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

Note 5: Uniformity measurement shall be taken at the locations shown in FIG. 14, for a total of the measurements per display, measure surface luminance of these nine points across the LCD surface 50cm from the surface with all pixels displaying white.

$$\text{Uniformity } \Delta Y = \frac{\text{Minimum Luminance of 9 points}}{\text{Maximum Luminance of 9 points}} \times 100\ (\%)$$

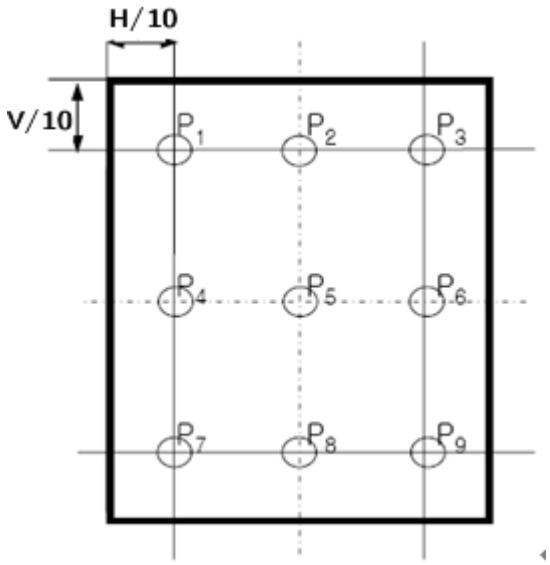


Figure 14: Uniformity Measurement Locations

Note 6: Image sticking

Condition: 65degC, 1hr,Test pattern: 5x5 Chess,Inspection pattern: 50% grey.<= Level 2.

Quantity:4PCS.

Result: Figure 15

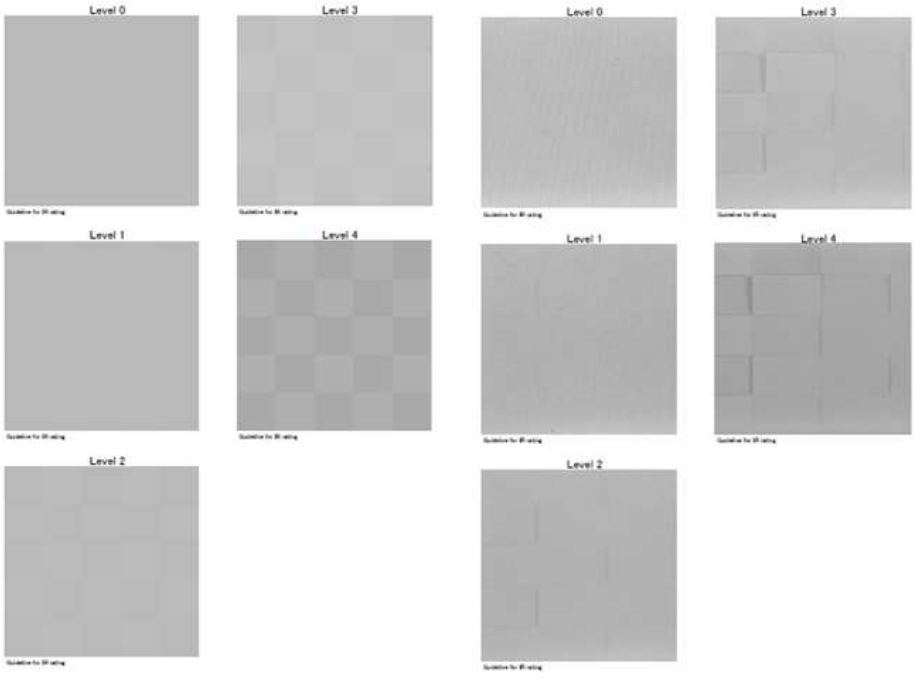


Figure 15

7. Reliability Tests / Environmental

7.1 Reliability Test Conditions

Table 11: List of reliability tests

Test		Symbol	Condition	Reference	Quantity
1	High Temperature Storage	HST	+95°C / 500 hrs	IEC 60068-2-2 Bb	4pcs
2	Low Temperature Storage	LST	-40°C / 500 hrs	IEC 60068-2-1 Ab	4pcs
3	High Temperature Operating (Note 1)	HOT	+85°C / 500 hrs	IEC 60068-2-2 Bb	4pcs
4	Low Temperature Operating	LOT	-40°C / 500 hrs	IEC 60068-2-1 Ab	4pcs
5	Accelerated Humidity Test Operating	AHTO	+60°C / 90% RH / 500 hrs	IEC60068-2-78 Cab	4pcs
6	Temperature Shock Test	TST	-30°C <> +85°C, 30min/5min/30min,100cycles Non-Operating	IEC 60068-2-14Na	4pcs
7	UV exposure resistance	UV	1KW Xenon/ 100 hrs Power off.	IEC 60068-2-5 Sa	2pcs
8	Mechanical Shock (Note 2)	-	3 directions: X,Y,Z axes Repeats:6 Peak acc.:10 G Pulse duration: 6 ms (half sine wave) Non-Operating	IEC 60068-2-27Ea	2pcs
9	Mechanical Vibration (Note 2)	-	3 directions: X,Y,Z axes Sweep time:10 (1Oct/ min) Frequency:10 -> 150->10 Hz 10-58 Hz: constant amplitude 0.75mm peak. 58-150Hz: constant acceleration 10g peak Sinusoidal, Non-Operating	IEC 60068-2-6Fc	1box

Note 1: Panel surface temperature should not exceed 95ºC.

Note 2: No optical performance guarantee below -30°C.

Note 3:For module internal structure robustness test purpose only. Customer application design should take care of overall mounting robustness with module.

7.2 Electrostatic Discharge (ESD)

Table 12: ESD test conditions

Test	Condition	Method	Remark	Quantity
Human body model	R = 330Ω, C = 150pF, • Air discharge: ±15 KV to display surface • Contact discharge: ±8 KV to metal frame	IEC61000-4-2	Not operating	2pcs
Machine model	R = 0Ω, C = 200pF, ±200V to I/O pins	MIL-STD-883, method 3015	Not operating	2pcs

Note 1: The TFT-LCD panel and IC on module are sensitive to electrostatic discharge. Please make sure equipment and operators are properly ground before during handling.

Note 2: As different customer application have different interfacing designs and assembly processes, the display module has no ESD protection circuitry. Customer is required to take special care on ESD level control in the assembly and test processes.

8. Inspection Criteria

8.1 Inspection Conditions

Table 13: List of inspection conditions and test pattern

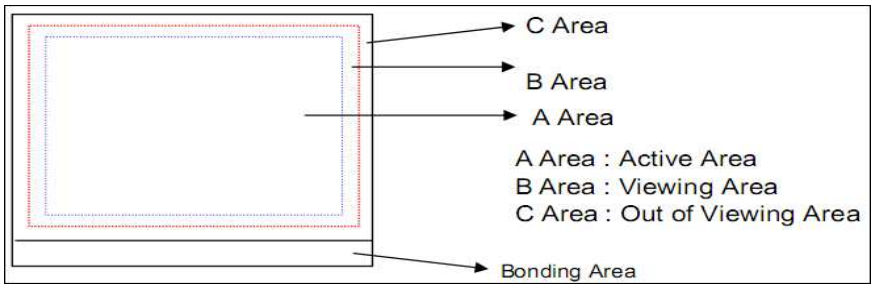
Item 项目	**Condition** 条件	
Ambient lighting 环境亮度	Non-operating inspection 800~2000 Lux. Operating inspection < 100 Lux. 非操作检查 800~2000 Lux. 操作检查< 100 Lux.	
Temperature /Humidity 温度/湿度	21 ± 4°C with 35~80%	
Driving condition 驱动条件	Equipment 设备	Product specific test tool 产品规格书说明的测试工具
	Test pattern 测试画面	Black, White, Red, Green, Blue, etc 黑, 白, 红, 绿, 蓝, etc
	Supply voltage 电源	Typical voltages as given in the specification 规格书提供的典型电压
Inspection method 检查方法	Time 时间	≤ 20 seconds ≤ 20 秒
	Distance 距离	35 cm ± 5 cm from display 距显示屏 35 cm ± 5 cm
	Viewing angle 视角	Standard viewing angle of inspection shall be perpendicular to the display. Inspection at other viewing angles shall not exceed 30° of perpendicular viewing angle. 视角检查的标准应垂直显示屏。其他视角检查范围应不超过垂直视角的 30°。

8.1.1 Dot and Line Defect Criteria 点型及线型不良标准

Table 14

Items 项目	Details 详细检查点		Inspection Criteria 检验标准
Sub Pixel Defects 子像素缺陷	Bright Sub Pixel Defect 亮子像素缺陷		N ≤0
	Dark Sub Pixel Defect 暗子像素缺陷		N ≤5,DS⩾10mm
	Joint Sub Pixel Defect (dark dot) 子像素相连缺陷(暗点)		N =1
	Bright + Dark Sub Pixel Defect 亮+暗子像素点缺陷		N ≤5 DS⩾10mm
Line Defects 线缺陷	Bright Line, Dark Line 亮线,暗线		N =0
Displayed Screen 显示区屏幕	Foreign material /Black/Bright Spot 异物黑/亮点 (Hair, Lint, etc) (头发，棉绒等)	Circular Type 圆型	D≤0.15,ignore
			0.15mm<D≤0.2mm, N≤3, DS>10mm
			0.2mm<D≤0.3mm, N≤2，DS>10mm
			D>0.3mm, N=0
		Linear Type 线型	W⩽0.05mm, Ignore 忽略
			0.05mm<W≤0.08mm, L≤3mm, N≤3, DS>10mm
			W>0.08mm, N=0
			L>3 mm, N=0
	Polarizer dent or bubble 偏光片凹痕、气泡	Circular Type 圆型	D≤0.15,ignore
			0.15mm<D≤0.2mm, N≤3, DS>10mm
			0.2mm<D≤0.3mm, N≤2，DS>10mm
			D>0.3mm, N=0
	Scratch 划痕	Linear Type 线型	W⩽0.05mm, Ignore 忽略
			0.05mm<W≤0.08mm, L≤3mm, N≤3, DS>10mm
			W>0.08mm, N=0
			L>3 mm, N=0
	Abnormal display 异常显示	All white 全白	Not allowed 不允许
		All black 全黑	Not allowed 不允许
		Gray scale 灰阶	Not allowed 不允许
		Abnormal display 异常显示	Not allowed 不允许
	Mura, 不均匀. (Pure black/with pattern check 纯,黑/白画面检查),		Refer to Domestic brands limit sample or 5%ND Filter 参考极限样品或者在 5% ND 滤片下检查，检查时间<3s。

Note 1) Definition of the Area 区域定义



Active Area:有效区域

Viewing Area:可视区域

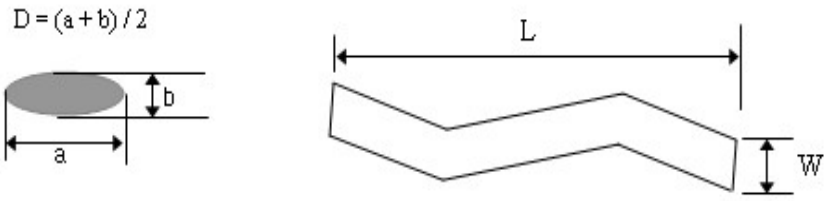
Out of Viewing Area: 可视区之外

Bonding Area: 邦定区域

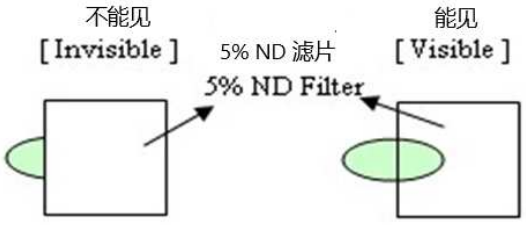
Note 2) D = Diameter (直径), L = Length(长度), W = Width (宽度), N = Number (数量), DS = Distance(距离)

Not included area: Glass edge to within 2mm area

不包含区域：玻璃边缘向内 2mm 的范围

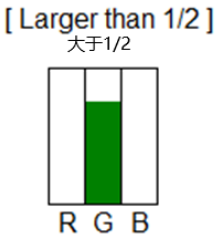


Note 3) Dot which is invisible through 5%ND filter or smaller than 1/2 of sub-pixel size will not counted as "1 dot"defect. 5%ND不可见或者小于1/2子像素大小的点不计算为“1点”缺陷.

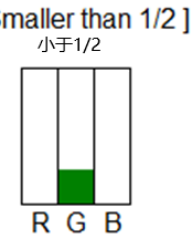


"No dot defect"
“没有不良点”
(=ignored/not counted)
不计算

"1 dot defect"
“1 个不良点”
(=counted)
计算

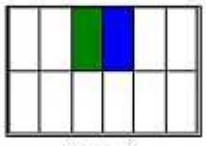


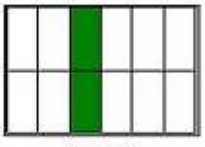
"1 dot defect"
“1 个不良点”
(=counted)
计算

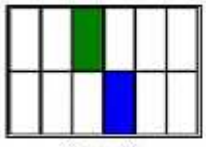


"No dot defect"
“没有不良点”
(=ignored/not counted)
不计算

[2 adjacent dots defect]
两个相邻亮子像素缺陷

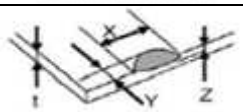
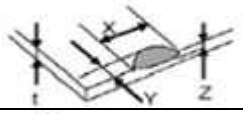
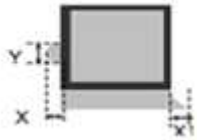






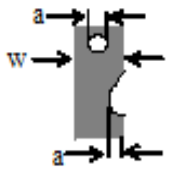
8.1.2 Appearance Inspection Criteria

Table 15

Defects 缺陷		Criteria 标准	Type 类型
Crack 裂纹		Not Allowed 不允许	Major 重要
CF Side Chipping CF 边崩裂		Y≤1/2 BM X Ignore 忽略 Z≤t	Minor 次要
TFT Side Chipping TFT 边崩裂		Y≤1mm X Ignore 忽略 Z≤t	Minor 次要
Corner Chipping 边角崩裂		X+Y≤4mm Z≤t	Minor 次要
Burr 毛刺		X+X1≤0.2mm 不影响功能、画面及组装	Minor 次要

8.1.3 FPC Defects FPC 缺陷

Table 16: FPC defect

Items 项目	Size (mm) 尺寸	Acceptance criteria 验收标准
FPC defect FPC 缺陷 	Dent, Pinhole a ≤ w/3 凹痕，针孔	No count 不计数
	Open circuit 开路	0
	Golden finger Oxidation, inerasable contamination 金手指氧化、擦不掉的玷污、	0

8.1.4 Other Cosmetic Defects(operating) 其它外观不良

Table 17: Other cosmetic defect

Items 项目	Criteria of acceptance 验收模式	Inspection pattern 检查模式
Residual shadow 拖影残留	Less than 3 seconds 持续少于3秒	All patterns 所有检测画面
Light leakage 漏光	Not visible in 30° viewing cone 30° 视锥内检查不出来	Pure white/Pure black 纯白/纯黑

Remark:

1. 以上均不得影响线路功能及组装
2. 表面脏污及黏着可擦拭为 OK

8.2 Malfunctioning

Not allowed are:

- Malfunctioning display: no picture, distinct block or line failure
- Malfunctioning backlight
- Excessive start up time > 3 seconds

8.3 Appearance

Not allowed are:

- Type and/or serial number (if any) wrong, missing or not legible
- Offensive surface damage
- Connectors damaged
- Stains within active area, such as fingerprints or adhesive residuals
- Dirty appearance (cannot be removed with a dry cloth)

8.4 Packing

Not allowed are:

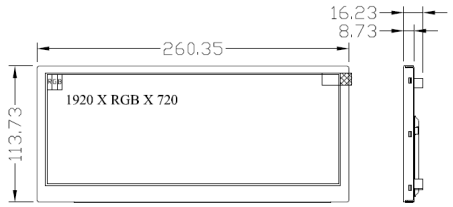
- Box damaged wet, badly taped or stapled causing the product not arriving in good condition at the customer
- Type or model number wrong (if any), missing or not legible

9. Packing Specification

PD DRAWING IS BASED COG-TA25F325P-L1,ONLY THE MODULE IS DIFFENENT.

CONFIGCURATION

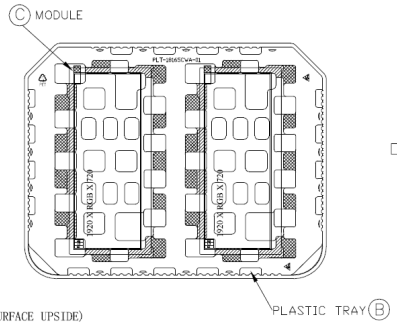
MS: COG-TA25F325P-L5 R0-20180928A



REV	AMENDMENT	DATE

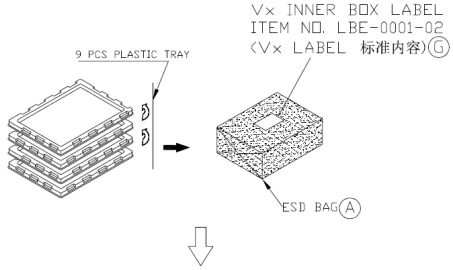
NO.	ITEM NO.	DESCRIPTION	QTY /BOX	BAAN UNIT	BOM DOSAGE	SIZE
K	CTN-315002002-01	HARD EDGES	2	PCS	0.0079	800×60×60
J	CTN-394002002-01	HARD EDGES	2	PCS	0.0079	1000×50×50
I	MPM-PALETTE-09	PALLET	1	PCS	0.0040	1200X1000
H	CTN-488002002-01	HARD EDGES	4	PCS	0.0157	1240×60×60
G	LBE-0001-02	INNER BOX LABEL	16	PCS	0.0625	102X36
F	LBE-102054-01	OUTER BOX LABEL	16	PCS	0.0625	102X54
E	SPE-VLBOT004-01	EPE BOARD	32	PCS	0.125	480X380X140
D	CTN-197158118K	OUTER BOX	16	PCS	0.0625	500X400X300
C	COG-TA25F325P-L5	MODULE	256	PCS		260.35X113.73X16.23
B	PLT-18165CWA-01	PLASTIC TRAY	144	PCS	0.5625	420X328X30
A	ESD-700615-01	ESD BAG	16	PCS	0.0625	700X615

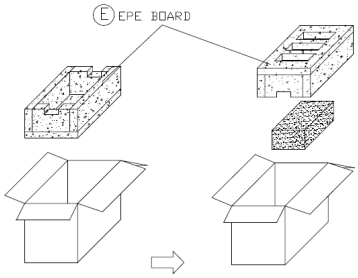
PLASTIC TRAY
ONE TRAY FOR 2 PCS MODULE
ITEM NO.: PLT-18165CWA-01
MATERIAL:TRANSPARENT PET T=1.2mm
PLASTIC TRAY SIZE: 420(L) X 328(W) X 30(H)mm



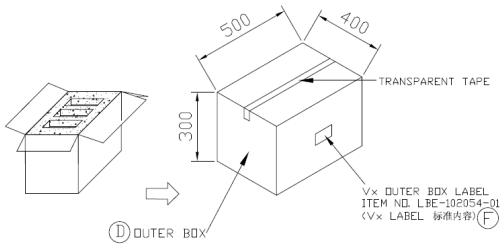
(DISPLAY SURFACE UPSIDE)
(显示屏朝上)

1. 2 PCS/TRAY X 8 TRAYS/OUTER BOX = 16 PCS/OUTER BOX.
2. EMPTY TRAY ADD ON TOP FOR ANTI-STATIC PURPOSE.
   (最上层吸塑盘为空盘)
3. EACH TRAY SHOULD BE ROTATED 180°.
   (每层吸塑盘需旋转180度摆放)
4. AFTER PUT THE TRAY INTO VACUUM BAG, SEAL THE OPENING BY TRANSPARENT TAPE
   (把吸塑盘装入ESD袋后再用透明胶纸封住)





OUTER BOX ITEM:CTN-197158118K

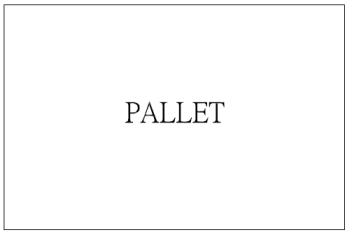


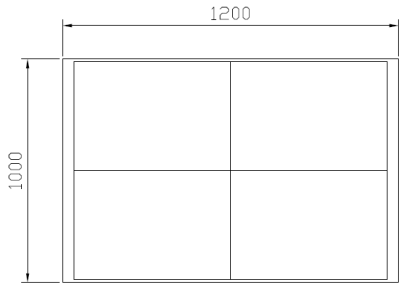
OUTER BOX

1. 2 PCS/TRAY X 8 TRAYS/OUTER BOX = 16 PCS/OUTER BOX.
2. PUT THE TRAYS WITH VACUUM BAGS INTO THE OUTER BOX
   (把吸塑盘装入纸箱)
3. EACH BOX SHOULD BE PLACED AN EPE BOARD ON THE TOP & BOTTOM.
   (每个纸箱的最上面&最下面须各放1块珍珠棉框)

TITLE: PACKING DRAWING				BOE	VARITRONIX LIMITED	
3rd ANGLE PROJECTION		UNIT: mm	SCALE: NOT TO SCALE			
	NAME	SIGN	DATE	MODEL: COG-TA25F325P-L5	REV	DATE
DRAWN	DENG WEN HAO				0	2019.7.25
CHECKED	ALISA ZHAO			DRAWING NO.: PD-COG-TA25F325P-L5 R0-20190725A		
APPROVED					SHEET 1 OF 2	

PALLET: MPM-PALETTE-09

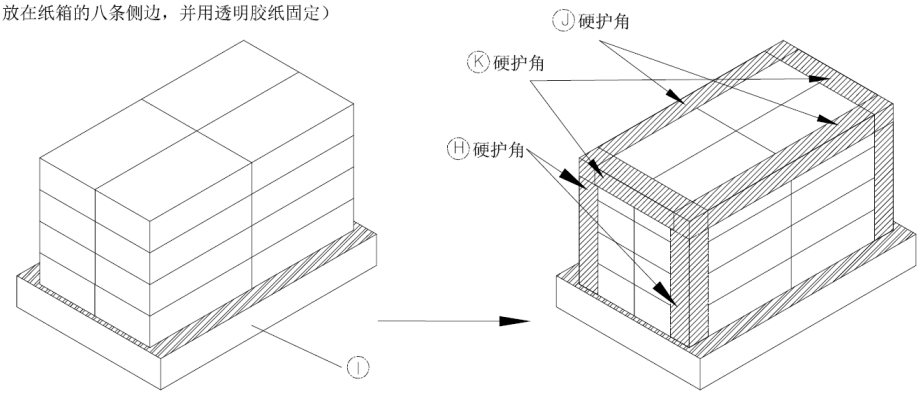




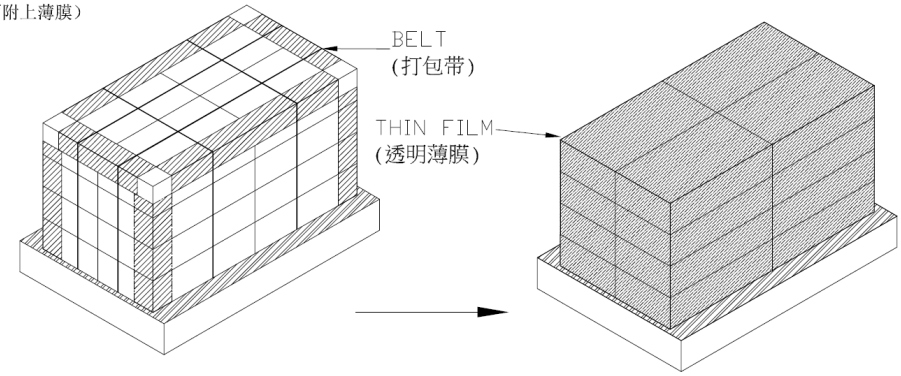
> 4 BOXES PER LEVEL (每层放4个BOX)
> 4 LEVEL PER PALLET (每卡板放4层)

2PCS/TRAY X 8TRAYS/BOX X 4 OUTER BOX/LEVEL X 4 LEVEL/PALLET = 256 PCS/PALLET.

1.STACK THE CARTON BOXES ON THE PALLET.
(把纸箱放在卡板上)
2.PUT THE HARD EDGES ON THE EIGHT SIDES, USE TRANSPARENT TAPE TO FIX.
(把纸护角放在纸箱的八条侧边，并用透明胶纸固定)



3. WRAP THE CARTONS BOXES WITH BELTS ON THE PALLET.
(用打包带将纸箱及卡板包扎好)
4.USE THE THIN FILM TO WRAP ALL THE CARTON BOXES.
(纸箱外面附上薄膜)

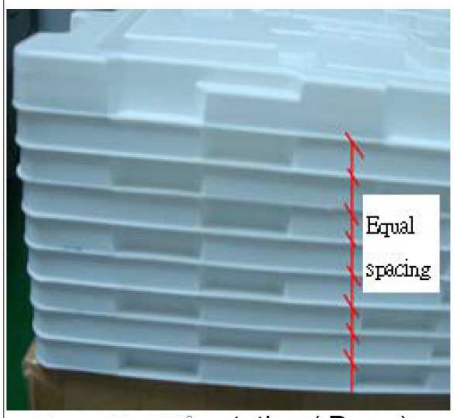
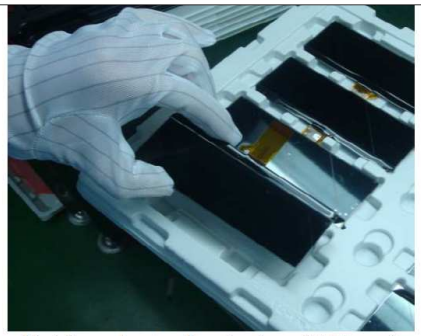
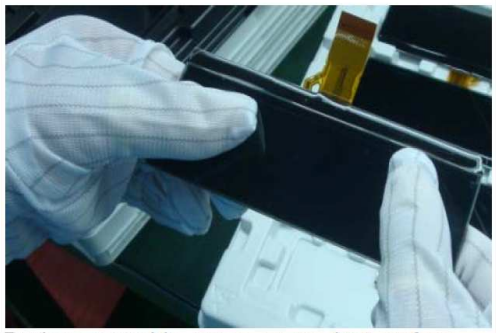
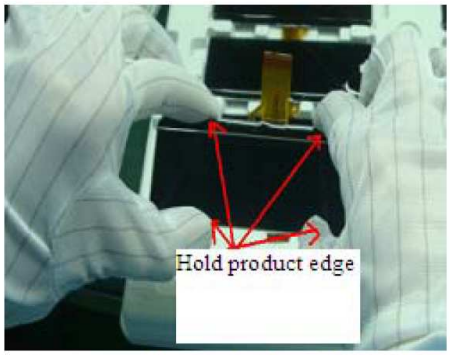


TITLE: PACKING DRAWING				BOE	VARITRONIX LIMITED		
3rd ANGLE PROJECTION		UNIT: mm	SCALE: NOT TO SCALE				
	NAME	SIGN	DATE	MODEL: COG-TA25F325P-L5		REV	DATE
DRAWN	DENG WEN HAO					0	2019.7.25
CHECKED	ALISA ZHAO			DRAWING NO.: PD-COG-TA25F325P-L5 R0-20190725A			
APPROVED						SHEET 2 OF 2	

10. Handling Cautions

10.1 Packing removal and handling requirement

Requirement	Wrong	Correct
Get one package each times & hold the package by both hands with proper ESD shielding	 Hold the modules by one hand and without proper ESD shielding (Fail)	 Hold the modules by both hands (Pass)
Prohibit to stack inner package over 3 layers	 Over 3 layers (Fail)	 Not exceed 3 layers (Pass)
Total packing tray height must within 40 cm	 Over 40 cm (Fail)	 Lower than 40 cm (Pass)

Requirement	Wrong	Correct
Packing tray must rotate 180° in each layer when stack together	 Tray without 180° rotation, It will have pressure on the module (Fail)	 Tray with 180° rotation (Pass)
Prohibit to touch product surface by fingers	 Hold product and touch its surface (Fail)	 Hold product edge by hand (Pass)
During assembly, prohibit to press on product surface by fingers, Must hold the product edges by both hands	 During assembly, press on product surface (Fail)	 During assembly, use both hands to hold Product edge only (Pass)

10.2 Mounting of module

- Please power off the display module before it is disconnected or connected to the application.
- If the connection to the application is not good, following problems may result.
  1. Significant noise on signals between display module and application
  2. Unstable display performance
  3. Parts on the module will be heat up or damaged
- The LCD module must be handled with care.
- Protective film (Laminator) is applied on surface for protection against scratches and dirts. Please avoid electrostatic charge build-up when peeling off the laminator.

10.3 Precautions in Mounting

- When metal part of the LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- Wipe off water drops or finger grease immediately when found. Prolonged contact with water may cause discoloration or spots.
- The LCD module contains glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- The display and IC on module are sensitive to electrostatic discharge; please make sure equipments and operators are properly ground before and during handling.

10.4 Adjusting module

- Adjusting volumes on the rear face of the module have been set to its optimal before shipment. Therefore, do not change any adjusted values. If adjusted values are changed, the display may not perform to specification.

10.5 Others

- Do not expose the module to direct sunlight or intensive ultraviolet rays for prolonged hours
- Store the module at room temperature condition.
- If LCD panel breaks, liquid crystal may escape from the panel. Avoid bringing it to eyes or mouth contact. When liquid crystal sticks on hands, clothes or feet, wash it out immediately with soap.
- Observe all other precautionary requirements as in handling general electronic components.
- Please adjust the voltage of common electrode as materials of attachment by 1 module.
- Do not expose the display module to harmful gases such as acid and alkali gasses, which will corrode electronic components.
- Do not disassemble the display module because it can cause permanent damage and will void the warranty agreement.

11. Definitions

Data sheet status	
Objective Specification	This data sheet contains target or goal specifications for product development.
Preliminary Specification	This data sheet contains preliminary data; supplementary data may be published later.
Product Specification	This data sheet contains final product specification.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating. Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operating of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Expose to limiting values for extended periods may affect device reliability. Device is functional within the limiting conditions doesn't imply the same performance over the covered conditions, customer is required to decide the best range for the final applications.	

12. Life Support Applications

These products are not designed for use in life saving appliances, devices or systems where malfunctioning of these products can reasonably be expected to result in personal injury. Customers using or selling these products for use in such applications do so at their own risk and agree full non liability of Varitronix Limited for any damages or losses resulting from such improper use or sale.