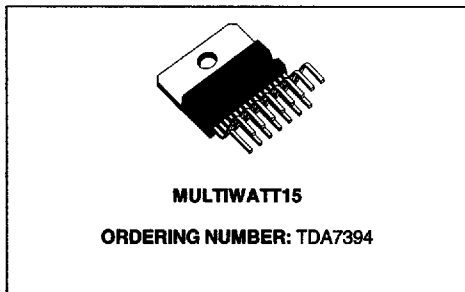


2 x 30W DUAL BRIDGE CAR RADIO AMPLIFIER

- **HIGH OUTPUT POWER CAPABILITY:**
 - 2 x 30W max./4Ω @ 13.2V, 1KHz
 - 2 x 22W typ./4Ω @ 14.4V, 1KHz, 10%
 - 2 x 19W typ./4Ω @ 13.2V, 1KHz, 10%
 - 2 x 28W typ./2Ω @ 14.4V, 1KHz, 10%
 - 2 x 25W typ./2Ω @ 13.2V, 1KHz, 10%
 - **LOW DISTORTION**
 - **LOW OUTPUT NOISE**
 - **ST-BY FUNCTION**
 - **MUTE FUNCTION**
 - **AUTO-MUTE AT MIN. SUPPLY VOLTAGE DETECTION**
 - **LOW EXTERNAL COMPONENT COUNT**
 - INTERNALLY FIXED GAIN (40dB)
 - NO EXTERNAL COMPENSATION
 - NO BOOTSTRAP CAPACITORS
 - **ADDITIONAL MONO INPUT**
- PROTECTIONS:**
- **OUTPUT AC/DC SHORT CIRCUIT TO GND AND TO V_s**
 - **VERY INDUCTIVE LOADS**
 - **OVERRATING CHIP TEMPERATURE WITH SOFT THERMAL LIMITER**
 - **LOAD DUMP VOLTAGE**

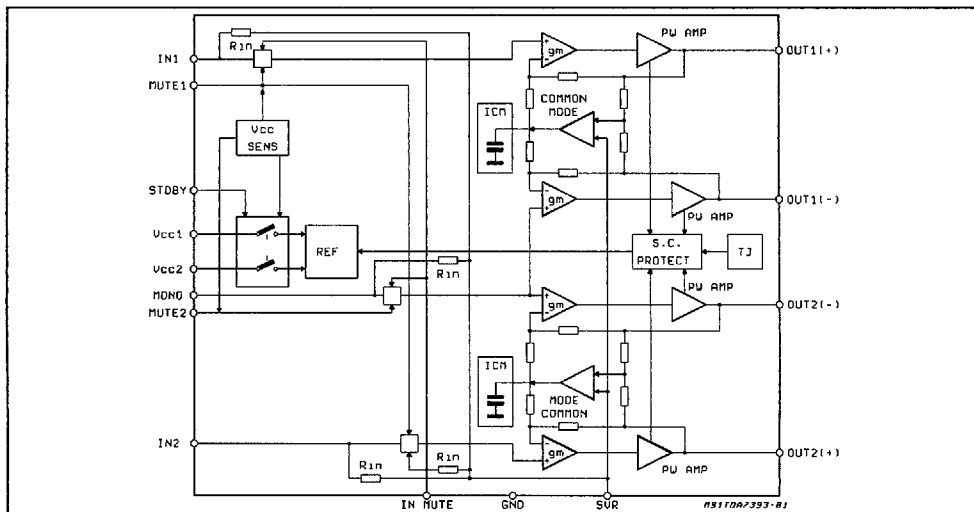


- **FORTUITOUS OPEN GND**
- **REVERSE BATTERY**
- **ESD PROTECTION**

DESCRIPTION

The TDA7394 is a new technology class AB Audio Power Amplifier in Multiwatt15 package designed for high end car radio applications. Thanks to the fully complementary PNP/NPN output configuration the high power performances of the TDA7394 are obtained without bootstrap capacitors. The extremely reduced components count allows very compact sets.

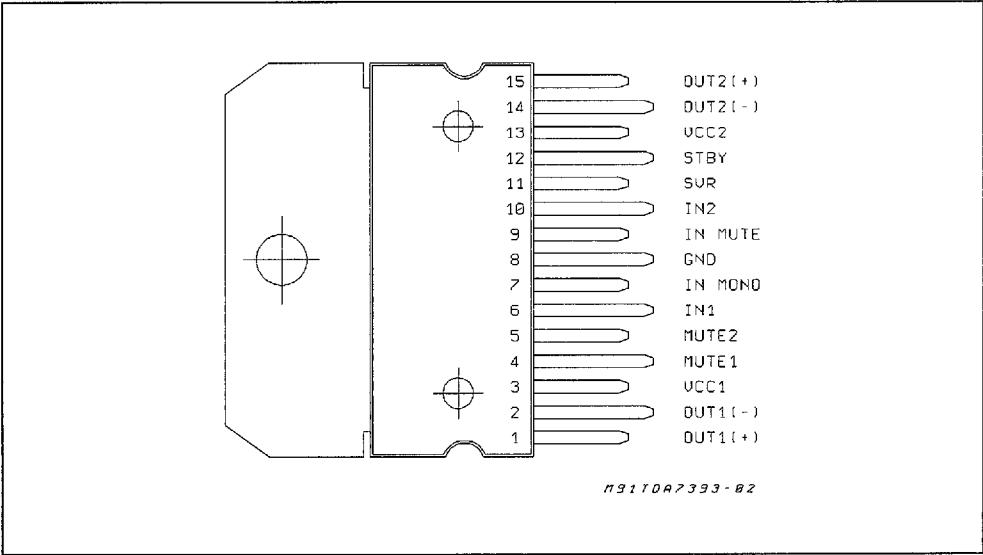
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Operating Supply Voltage	18	V
V _{CC} (DC)	DC Supply Voltage	28	V
V _{CC} (pk)	Peak Supply Voltage (t = 50ms)	50	V
I _O	Output Peak Current: Repetitive (Duty Cycle 10% at f = 10Hz) Non Repetitive (t = 100µs)	4.5 5.5	A A
P _{tot}	Power dissipation, T _{case} = 75°C (see derating curve)	50	W
T _J	Junction Temperature	150	°C
T _{op}	Operating Ambient Temperature	− 40 to 85	°C
T _{stg}	Storage Temperature	− 55 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th j-case}	Thermal Resistance Junction to Case	Max. 1.5	°C/W

7929237 0064839 847

ELECTRICAL CHARACTERISTICS ($V_S = 13.2V$; $f = 1KHz$; $R_g = 600\Omega$; $R_L = 4\Omega$; $T_{amb} = 25^\circ C$;
Refer to the application circuit, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{q1}	Quiescent Current			90	180	mA
V_{OS}	Output Offset Voltage		- 200		+ 200	mV
G_v	Voltage Gain		38.5	40	41.5	dB
P_o	Output Power	THD = 10%; $V_S = 14.4V$ THD = 10% THD = 1% THD = 10%; $R_L = 2\Omega$ THD = 10%; $V_S = 14.4V$; $R_L = 2\Omega$	17	22 19 16 25		W W W W
$P_{o\ max}$	Max. Output Power	EIAJ RULES		30		W
THD	Distortion	$P_o = 4W$		0.08	0.3	%
e_{No}	Output Noise	$Bw = 20Hz$ to $20KHz$			0.5	mVrms
SVR	Supply Voltage Rejection	$f = 100Hz$ (stereo)		60		dB
f_L	Low Cut-Off Frequency			10		Hz
f_H	High Cut-Off Frequency			200		KHz
R_i	Input Impedance		10	15	20	K Ω
C_T	Cross Talk	$f = 1KHz$	50	65		dB
I_{SB}	St-By Current Consumption				100	μA
$V_{SB\ out}$	St-By OUT Threshold Voltage	Amp: ON	3.5			V
$V_{SB\ in}$	St-By IN Threshold Voltage	Amp: OFF			1.5	V
V_{SB}	Supply Dependent St-By Threshold	St-By = H, V_S reducing/increasing		7.5	8.3	V
A_M	Mute Attenuation	$V_O = 1Vrms$		75		dB
$V_{M\ out}$	Mute OUT Threshold Voltage	Amp: Play	3.5			V
$V_{M\ in}$	Mute IN Threshold Voltage	Amp: Mute			1.5	V
V_M	Supply Dependent Mute Threshold	Mute = IN, V_S reducing/increasing		8.5	9.3	V
$I_m (L)$	Muting Pin Current	$V_{MUTE} = 1.5V$ (Source Current)	6	10	14	μA
$I_m (H)$	Muting Pin Current	$V_{MUTE} = 3.5V$ (Source Current)	6	10	14	μA

Figure 1: Quiescent Current vs. Supply Voltage

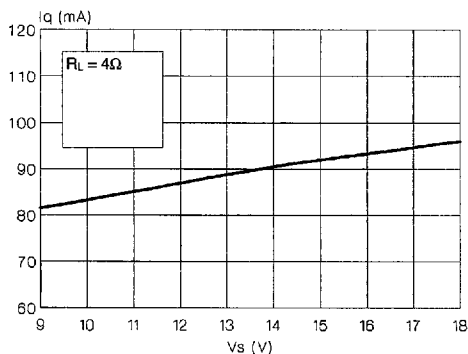


Figure 2: Output Power vs. Supply Voltage

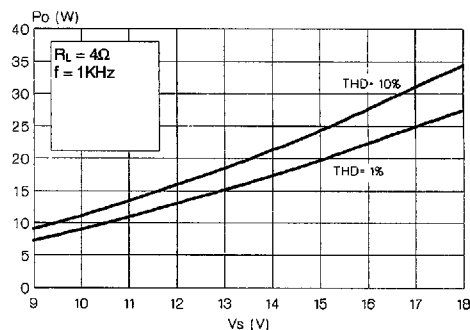


Figure 3: Output Power vs Supply Voltage

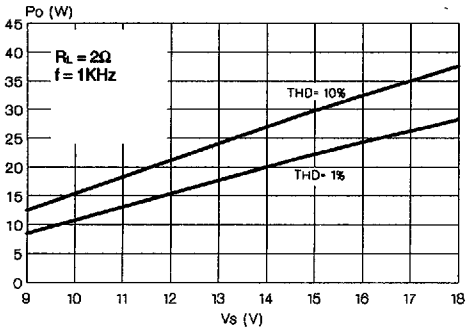


Figure 4: EIAJ Power vs. Supply Voltage

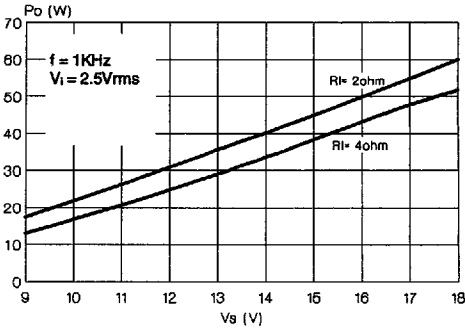


Figure 5: Cross-Talk vs. Frequency

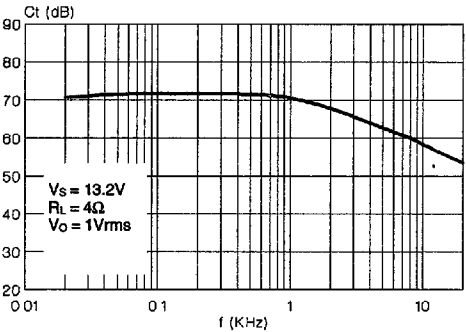


Figure 6: SVR vs. Frequency

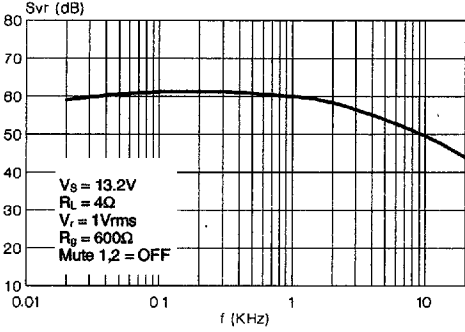


Figure 7: Distortion vs. Frequency

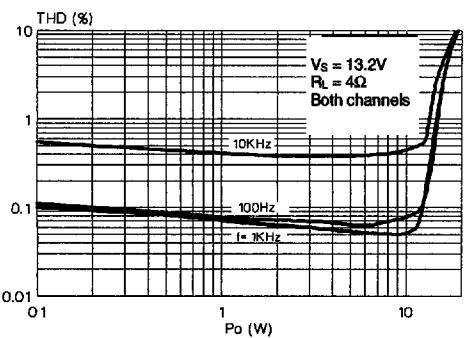


Figure 8: Distortion vs. Frequency

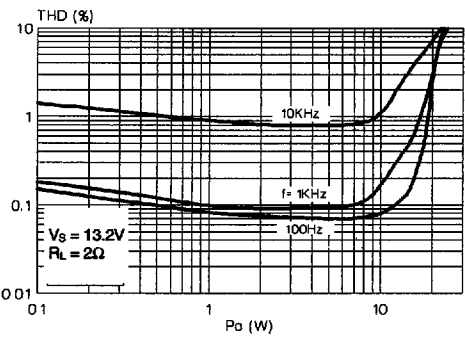


Figure 9: Block Diagram of Mute Circuit

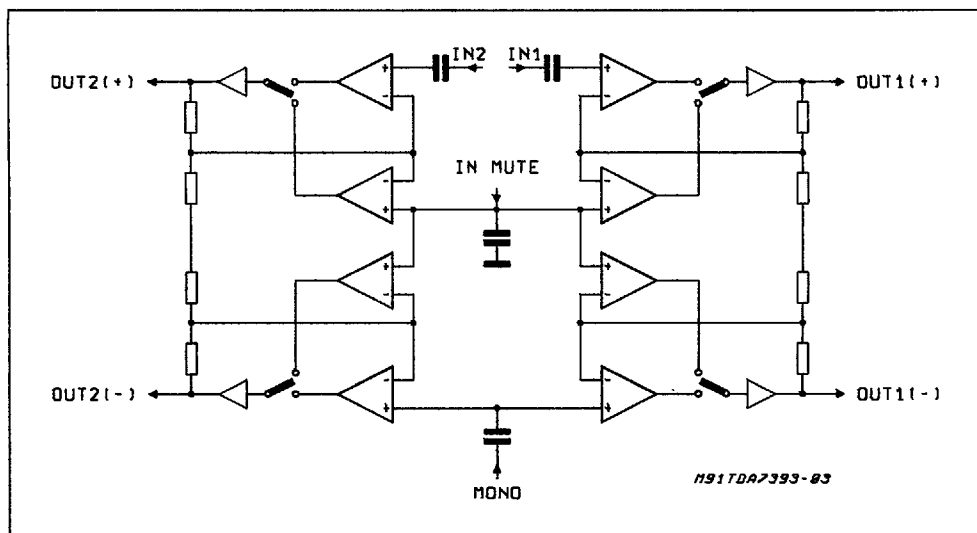


Figure 10: Explanatory Waveforms Of Mute Circuit

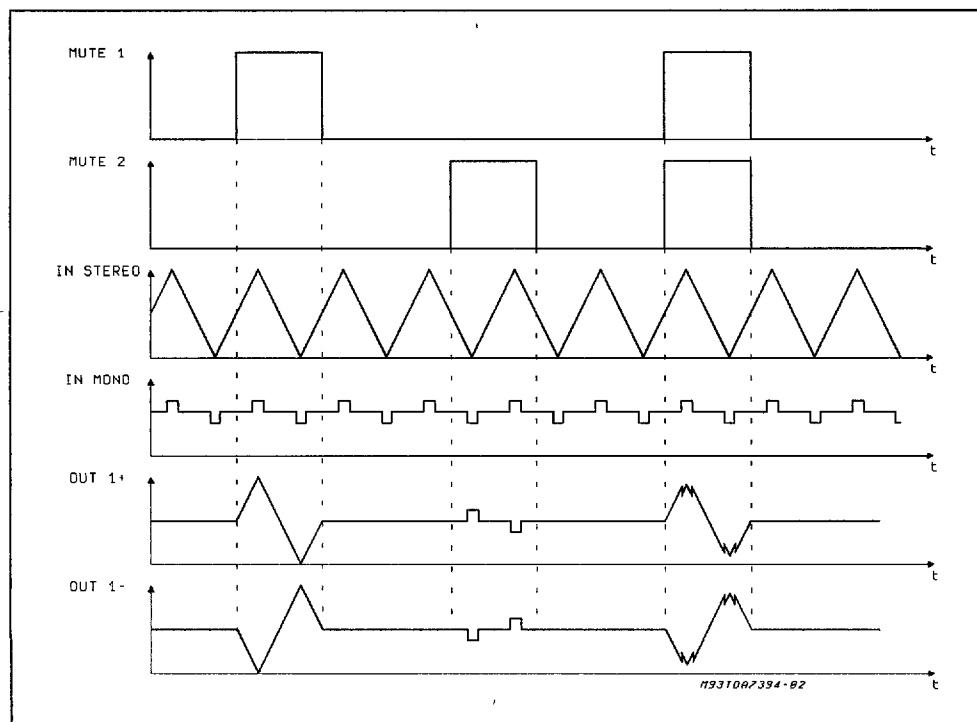


Figure 11: Application Circuit

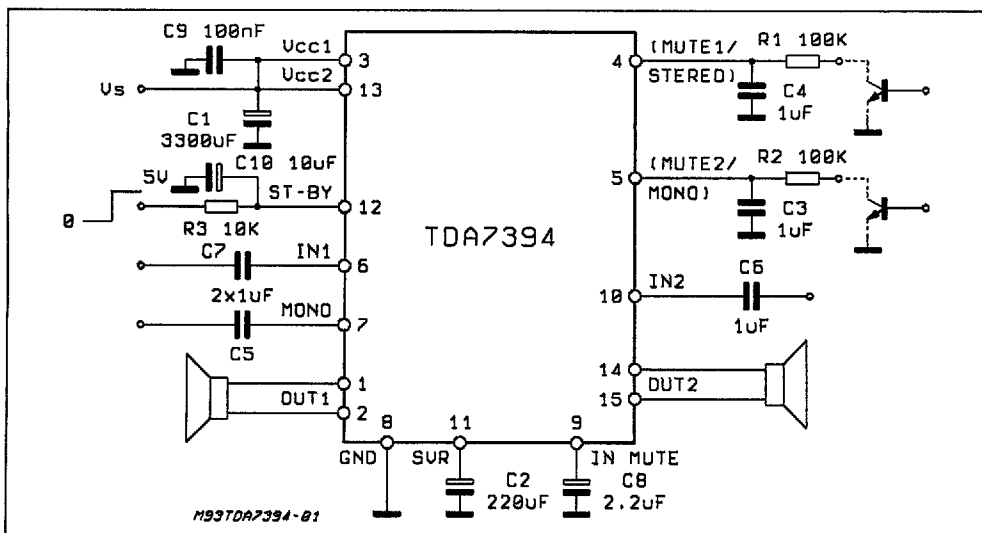


Figure 12: P.C. Board and Component Layout of the fig. 11 (1:1 scale)

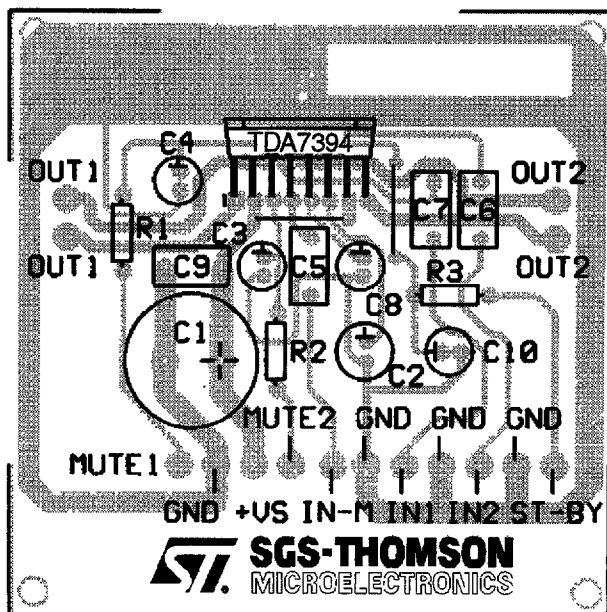
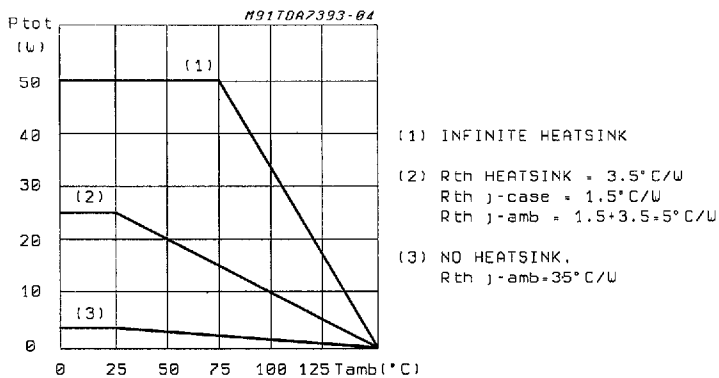


Figure 13: Power Dissipation Derating Curve



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